Claims

Sub C3

1. A circuit for input side impedance matching of a power amplifier in an electronic device, comprising:

a source for providing a signal, wherein the signal has a predetermined impedance; and

an impedance transformer network joined in parallel with the source, wherein the network comprises a negative resistor in series with an inductor, and wherein the network synthesizes the predetermined impedance at an input of the power amplifier.

2. The circuit of claim 1, wherein the inductor has a reactance equal to a capacitance of the device at a required frequency of operation.

3. The circuit of claim 2, wherein the inductor is a bondwire inductor.

4. The circuit of claim 1, wherein a value of the negative resistor is selected to synthesize the predetermined impedance at an input of the power amplifier.

5. The circuit of claim 4, wherein the value of the negative resistor is approximately -7.4 Ohms.

6. The circuit of claim 4, wherein the predetermined impedance is approximately 50 Ohms.

7. The circuit of claim 4, wherein a normalized phase of the synthesized impedance is between approximately -0.5 to 0.5 Radians.

8. The circuit of claim 7, wherein the normalized phase is approximately -0.4 Radians.

9. The circuit of claim 1, wherein a ratio of signal voltage at an input of the power amplifier to signal voltage at the source is approximately 0.62.

Sub B4

10. A circuit for input side impedance matching of a power amplifier in an electronic device, comprising:

a source for providing a signal, wherein the signal has a predetermined impedance;

an impedance transformer network joined in parallel with the source, wherein the network comprises a negative resistor in series with an inductor; and

wherein a value of the negative resistor is selected to synthesize the predetermined impedance at an input of the power amplifier, and wherein the inductor has a reactance equal to a capacitance of the device at a required frequency of operation.

11. The circuit of claim 10, wherein the predetermined impedance is approximately 50 Ohms, and wherein the value of the negative resistor is approximately –7.4 Ohms.

12. The circuit of claim 11, wherein the synthesized impedance has a normalized phase between approximately -0.5 and 0.5 Radians.

13. The circuit of claim 12, wherein the normalized phase is approximately -0.41 Radians.

14. The circuit of claim 13, wherein a ratio of signal voltage at the input to signal voltage at the source is approximately 0.62.

Sub A5

15. A method for matching impedance at an input of a power amplifier in an electronic device, comprising the steps of:

providing a signal from a source, wherein the provided signal has a predetermined impedance;

joining an impedance transformer network in parallel with the source, wherein the network comprises a negative resistor in series with an inductor; and

selecting a value for the negative resistor so that the predetermined impedance is synthesized at the input of the power amplifier.

16. The method of claim 15, further comprising the step of setting a reactance of the inductor equal to a capacitance of the device at a required frequency of operation.

17. The method of claim 15, wherein the selecting step comprises selecting a value of -7.4 Ohms for the negative resistor.

18. The method of claim 15, wherein the predetermined impedance is approximately 50 Ohms.

19. The method of claim 15, wherein a normalized phase of the synthesized impedance is approximately -0.41 Radians.

20. The method of claim 15, wherein a ratio of signal voltage at the input to signal voltage at the source is approximately 0.62.